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10/644,561	08/19/2003	Hsueh-Yuan Pao	IL-11028	6617

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EXAMINER	
VARTANIAN, HARRY	
ART UNIT	PAPER NUMBER
2634	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,561	PAO ET AL.	
	Examiner	Art Unit	
	Harry Vartanian	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/2003, 02/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In para 0020(PG-PUB version) there is a typo in the line that reads "XDSL irefers..."

In para 0036(PG-PUB version) the line that reads "The registers 126 to 128" seems as though it should read "The registers 124 to 127".

Appropriate correction is required.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 110, 120, 201, 210, 215, 401, 410, 420, 430, 440, 450, 460, 470, 480, 1112-1114. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "200"(figure 3 and 5) and "201"(figure 6E) have both been used to

designate the end result of the modulation. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 1100. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claims 1-9, 11, and 12 are objected to because of the following informalities:

In claim 3, line 5 "wherein at least..." seems as though it should recite "wherein **said** at least one..." This also occurs in claims 5, 9, and 11.

In claim 5, line 2 "said at least one multiplexer" lacks antecedent basis.

In claim 7, line 11 "wherein said plurality of adders" lacks antecedent basis.

In claim 9, line 1 "said at least one multiplexer" lacks antecedent basis.

In claim 11, line 1 "said at least one multiplexer" lacks antecedent basis.

In claims 1-8 and 12 please change "QAM" in the preamble to "Quadrature Amplitude Modulation(QAM)".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 4, 6-8, 10, and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by Zhang(US PAT# 6,430,228). Zhang discloses a QAM modulator that uses lookup tables to map parallel data in order to reduce the number of multipliers. Regarding Claim 1, Zhang meets the following limitations of the claim:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data; **fig 1, item 21**

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations; **fig 2, item 47; (Column 5, lines 21-40)**

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q1 to Qx, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **fig 6B**

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and **(column 5, lines 10-46)**

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data. **(Fig 2, item 53)**

Regarding Claim 2, Zhang meets the following limitations of the claim:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data; **fig 1, item 21**

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations; **fig 2, item 47; (Column 5, lines 21-40)**

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_x, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **fig 6B**

a plurality of registers operatively connected to collect and shore said output data comprising IQ_1 to IQ_{IQN}; **(column 5, lines 10-46)**

at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN}; **fig 3b**

at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and **fig 3a**

a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data. **(Fig 2, item 53)**

Regarding Claim 4, Zhang meets the following limitations of the claim:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to I_N, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **fig 6B**

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; **(column 5, lines 10-20)**

a first multiplexer operatively connected to collect from said plurality of registers only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN}; **fig 3b**

a second multiplexer operatively connected to collect from said plurality of registers only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and **fig 3a**

a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data. **(Fig 2, item 53)**

Regarding Claim 6, Zhang meets the following limitations of the claim:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to $I_{N,}$, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **6B**

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and **(column 5, lines 10-20)**

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data. **(Fig 2, item 53)**

Regarding Claim 7, Zhang meets the following limitations of the claim:

receiving and converting a string of serial data into a plurality of parallel data; **fig 1, item 21**

determining the I and Q locations of said plurality of parallel data; **fig 2, item 47**

storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_N, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

receiving and adding said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders,

wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **6B**

collecting and storing said output data comprising IQ_1 to IQ_{IQN} in a plurality of registers; **(column 5, lines 10-20)**

converting said output data comprising IQ_1 to IQ_{IQN} to analog data in a digital to analog converter. **(Fig 2, item 53)**

Regarding Claim 8, Zhang meets the following limitations of the claim:

receiving and converting a string of serial data to a plurality of parallel data; **fig 1, item 21**

receiving said plurality of parallel data in an I and Q mapper and determine the I and Q locations of said plurality of parallel data; **Abstract; (Column 5, lines 21-40); fig 6B**

receiving and storing said I and Q locations in a plurality of look-up tables (LUTs), wherein the I LUTs are configured I_1 to I_N, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs; **6B**

receiving and adding said I and Q locations stored within said plurality of LUTs in a plurality of adders, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **6B**

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN}; **(column 5, lines 10-20)**

collecting, in a multiplexer, from said plurality of registers, the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN}; **fig 3b**

collecting, in a multiplexer, from said plurality of registers, the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and **fig 3a**

converting, a digital to analog converter, said odd subscript data and said even subscript data to analog data. **(Fig 2, item 53)**

Regarding Claim 10, Zhang meets the following limitations of the claim:

receiving and storing in a plurality of look-up-tables (LUTs), I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_x, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **6B**

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN}; **(column 5, lines 10-20)**

collecting in a first multiplexer only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN}; **fig 3b**

collecting in a second multiplexer only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and **fig 3a**

converting in a digital to analog converter said odd subscript data and said even subscript data to analog data. **(Fig 2, item 53)**

Regarding Claim 12, Zhang meets the following limitations of the claim:

receiving and storing, in a plurality of look-up-tables (LUTs) I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_x, wherein X is the highest number of Q LUTs of said plurality of LUTs; **Abstract; (Column 5, lines 21-40); fig 6B**

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said
6B

plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN}; **fig 6b**

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN}; **(column 5, lines 10-20)**

converting in a digital to analog converter said output data comprising IQ_1 to IQ_{IQN} to analog data. **(Fig 2, item 53)**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 3, 5, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang(US PAT# 6,430,228). Zhang meets all the limitations of claims 3, 5, 9, and 11(see above paragraphs) except disclosing the exact multiplexer configuration wherein nx2 multiplexers are used.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use various permutations of multiplexers since it is well-known in the art that there are multiple ways to translate multiple signals into one output. For instance, Zhang could use two 4x2 and two 2x1 multiplexers to substitute for one 8x1 multiplexer. In addition, applicant has not disclosed that nx2 multiplexers provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with one 8x1 multiplexer because it would reduce FPGA programming complexity. Therefore, it would have been obvious to one of ordinary skill in this art to modify Zhang to obtain the invention as specified in claims 3, 5, 9, and 11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Vartanian whose telephone number is 571.272.3048. The examiner can normally be reached on 10:00-6:30 Mondays to Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571.272.3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Harry Vartanian
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HV

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